REMARKS

Reconsideration of the application in view of the following remarks is respectfully requested.

The Examiner rejects Claims 2, 6-8 and 10-11 under 35 U.S.C. 103(a) as being unpatentable over Lim, prior art of record, in view of Hardy or Lofstrom, which are newly cited prior art. The Examiner refers to FIGURE 4 of LIM as showing a signal level detection comprising a first DC error amplifier operational to generate a control signal in response to a reference signal and a first inverter operation to generate the feedback signal in response to the first DC error amplifier control signal but does not show combining the two identical DC amplifiers receiving a differential input signal. The Examiner states that Hardy et al. and Lofstrom show that a differential output comparator can be formed by combining two identical amplifiers receiving a differential input signal. The Examiner concludes that one skilled in the art would recognize to modify Lim's circuit to use two identical amplifiers and suggested by Hardy et al. and Lofstrom.

The Examiner rejects claims 2, 6-8 and 10-11 under 35 U.S.C. 103(a) as being unpatentable over Lim et al., prior art of record, in view of Hardy et al. or Lofstrom. This rejection is similar to the above rejection except that it relates to FIGURE 1 of Lim et al.

We can not agree. Both Lim references relate to bipolar circuits. Obtaining sufficient bandwidth using bipolar circuits is relatively easy but very difficult using CMOS circuits, for example. The circuits of Lim in FIGURE 4 and Lim et al. in FIGURE 1 both utilize the same path for controlling the threshold voltage and for detecting the level of the input voltage. If this technique were applied to CMOS circuits, for example, the resulting circuits would have insufficient bandwidth for many applications. In sharp contrast, the present invention utilizes a separate loop having the inverter 12 for

establishing the threshold voltage at which the inverter is set. The same voltage is utilized to operate other inverters, such the inverter formed by transistors MP5, MN6 and MN5 in FIGURE 1. The second or signal inverter can then be operated in an open loop fashion to obtain the required bandwidth. Also, as illustrated in FIGURE 1, multiple inverter stages can be cascaded in order to provide the necessary gain to provide the signal level detection. In addition, the set points of the inverters can be adjusted so that they are at the linear portion of the inverter design, which produces maximum gain. Claims 2, 6 and 10 have been amended in this respect.

Accordingly, Applicants believe the Application, as amended, is in condition for allowance, and such action is respectfully requested.

Respectfully submitted,

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